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Design Optimization of an Electrowetting Cell Sorter Chip Platform

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Abstract

In this paper fast but simple physical sorting algorithms for high-volume cell sorting based on the microfluidic electrowetting platform are analyzed and further optimized. Relying on both, hardware demonstrations of the underlying sorting operators and simulations of different generic sorter topologies, first design studies for the realization of an efficient cell sorter chip platform are carried out.

1 Introduction

Electrowetting is known to be an applicable technology for the handling of cell suspensions [1-4]. The target processes of the droplet based handling by electrowetting, as shown in Image 1, can also be applied for sorting of cells by separating large droplet volumes of cell suspensions including intermediate dilution steps, down to the single cell. During processing the cells will be optically inspected and sorted according to the specifications. The application of the cell sorter chip platform will be in biomedical and clinical research as well as the early stage diagnostics of infectious and tumor diseases.

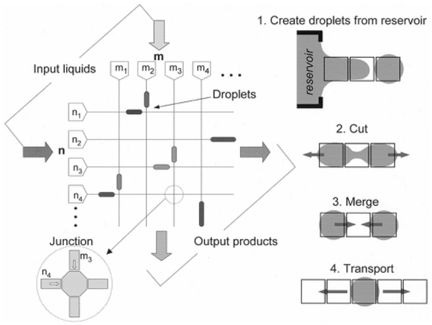


Image 1 Droplet operations on an electrowetting chip platform [2]

The main task of the physical sorting algorithm (an algorithm is realized by a corresponding microfluidic chip architecture) is to separate a specifically labeled cell type from a cell mixture. This generic “one-out-of-a-mixture” selection process has to be optimized for maximal cell throughput or maximal sorter efficiency (i.e. the relative amount of the end products) relying on specific operators such as generating, transporting, merging and dividing liquid droplets in the framework of electrowetting. Interestingly, there is virtually no literature available on scalable particle or cell sorter architectures, which means that one has to borrow concepts from alien disciplines such as e.g. logistics networks [5] and supply chain (and distribution) systems [6], though it does not dispense us from designing sorter concepts from scratch. Hence, owing to the complexity of the optimization task, any sorter chip design will therefore heavily depend on extensive numerical modeling together with tailored electrowetting chip design for the specific droplet manipulations. In the electrowetting chips the handling processes are verified and the timing is monitored. This allows a direct feedback into the modeling process for further optimization.

2 Methods

2.1 Sorting topology

2.1.1 Modeling physical sorting algorithms

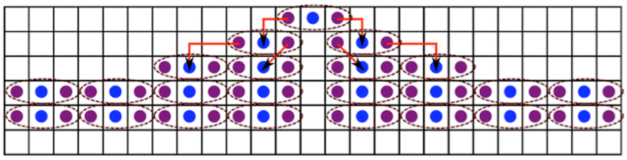
The simulation of the physical sorting process, namely the manipulation of corresponding droplets upon an electrode matrix (by electrowetting) and the associated graphical visualization is carried out using MATLAB [7]. The droplet consisting of a cell suspension (using e.g. PBS) is construed as a datum of information that refers to the droplet volume (typically 5.7 nl), the total number and the number of labeled cells. Hence droplet chains can be conceptualized as very particular “data streams” that are “clocked“ [according to a clock rate ranging from 10 Hz up to 10 kHz] along columns and rows of the sorter chip’s electrode matrix while undergoing various manipulations.
Due to the affinity between MATLAB’s matrix capabilities and the matrix layout of the electrowetting electrodes, the local droplet information can be easily assigned to a corresponding data matrix that is ready for further processing. The three main operators used for modeling the dynamics of droplet manipulation are transport, merging and splitting. In contrast to the first two operators, at which adjacent matrix elements are being assigned and rewritten accordingly to mimick the corresponding droplet motion, the splitting operator is more complex. A realistic splitting scenario has to consider the droplet volume and the amount of particles using a stochastic two-stage model

with probability mass functions according to a hypergeometric distribution.

2.1.2 Two generic sorter topologies

In order to support high-volume cell sorting the underlying algorithm has to be as simple as possible. Image 2 depicts two binary sorting schemes where the droplets are divided and refilled e.g. with PBS, and hence diluted down to levels, where the number of either the labeled cells or the residual cells within a droplet starts to dominate.

(a) Linear (binary) sorter topology



(b) Radial sorter topology

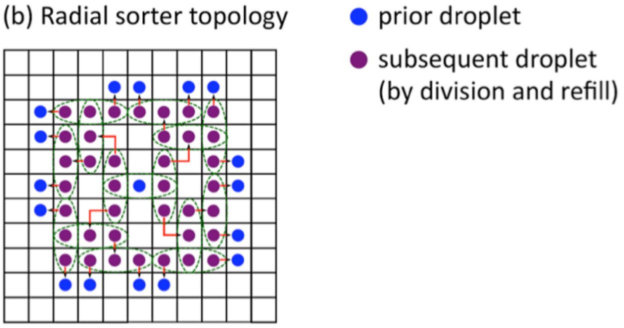


Image 2 Schematics of two generic cell sorter architectures that conform to the electrowetting electrode matrix.

This "number quantization effect" can be further exploited while manipulating and rearranging the droplets under optical inspection (regarding cell numbers) of the overall array with a highly sensitive camera, yielding droplets that contains either (one or more) labeled cells or residual cells only. The execution of the sorting process conforms to a binary tree as shown in Image 2(a), where the throughput of labeled cells (at the bottom) strongly depends on the composition of the suspension in the starting droplets (top) and predominantly on the horizontal extent of the electrode array. A first attempt to scale-up the performance is provided by the *radial sorter topology* shown in Image 2(b), which basically consists of four linear sorters attached to a center region (purple droplets only), which is solely responsible for the droplet distribution into the four sorter "arms".

Within a preliminary benchmark scenario we simulated the throughput of sorted cells per clock (cells/clock) for 100% sorter efficiency of both topologies implemented on a 25 × 25 electrode array starting with a suspension, where the ratio of labeled cells amounts to 50%. The *linear sorter* yields a steady-state throughput of 2.3 cells/clock and the radial sorter 3.0 cells/clock. The poor scaling behavior of the *radial sorter* (1.3-fold speed-up) is mainly due to the large coverage of the central region compared to the overall area and may be improved with increasing chip size. These two idealized models do neither account for a realistic PBS supply nor for a proper removal of the final droplets (with either labeled or residual cells), but they are fully capable to provide first qualitative estimates on performance, scaling behavior and potential bottlenecks in conjunction with particular sorter topologies.

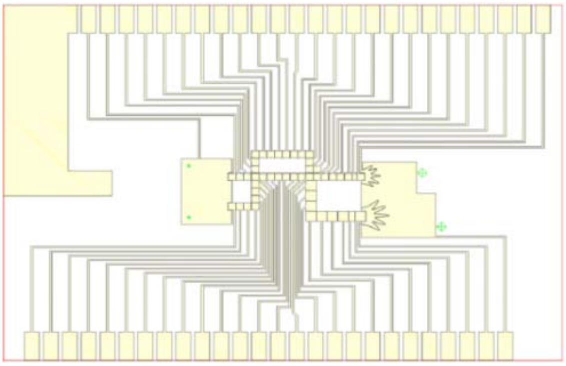
2.2 Electrowetting test chips

For verification of the required sorting steps as droplet generation, transportation, merging and splitting as a first approach simple electrowetting chips have been designed, build and tested concerning their general functionality and speed.

2.2.1 Chip design

As a first simple design an electrowetting chip has been realized with a single electrode activation with two rows of electrodes and two reservoirs, according to Image 4(a). The electrode dimensions are 500 x 500 mm and a pitch of 520 μm. The next design iteration, Image 4(b), is based on a 8 x 8 electrode matrix and four reservoirs. The electrodes have a size of 350 x 350 μm with a pitch of 370 μm. Bottom and top layer are separated by a 30 μm spacer foil. This yields in a droplet volume of approximately 5.7 nl. Two reservoirs are for the feeding of phosphate buffered saline (PBS) for dilution, one for the sample solution and one output reservoir, all with a size of 3 x 3 mm^2.

(a) single electrode activation design



(b) matrix design

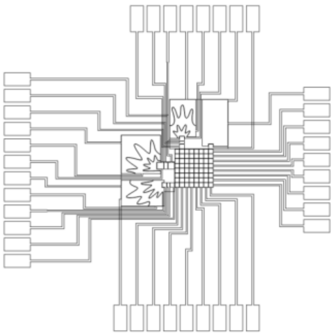


Image 3 Schematics of the electrowetting testing chip.

2.2.2 Materials, prototyping and testing of chip

The chip layout is a three layer system with a bottom and top layer from glass with a 100 nm thick coating with ITO. The electrodes are laser micro structured and then coated with a silicon oxide and silicon nitride dielectric layer (only bottom) and a hydrophobic Teflon coating. As third layer, a PET spacer foil between bottom and top layer with a thickness of 30 μm is used.

The testing of the chip is carried out with the cell carrier solution PBS and 0.003 % Tween. As second phase silicone oil is used. The experiments have been carried out without cells with a 43Vpp rectangular signal and a frequency of 1.4 kHz.

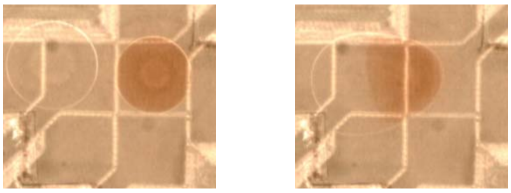
3 Results

3.1 Process verification on electrowetting chips

With the first electrowetting chip design [Image (3a)] the principal fluidic operations as the droplet generation, transportation, merging, mixing and splitting have been evaluated. For the droplet generation a speed of 3 s, for the transportation 2.5 mm/s and for the splitting 2 s are required.

For the mixing different methods can generally be applied. One method can be the up and down movement of the droplet on the linear electrode tracks. Alternatively the droplet can be rotated on a four electrode area. The mixing progress on a four electrode design is shown on Image 6. Experimental comparison of the two approaches exhibited that the circular rotation of the droplets is more efficient since less switching steps are required and a higher speed of around 5 s compared to 10 s in the linear mixing with the same mixing result can be achieved.

(a) separate droplets (b) fusion of droplets



(c) one mixing cycle (d) full mixing after six cycles

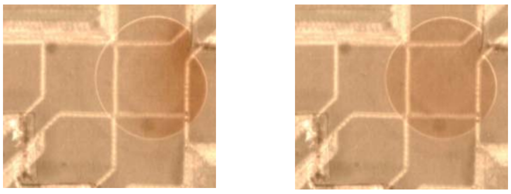


Image 6 Mixing progress on a four electrode design

Summing up the experimental analysis of the single processing steps it can be said that the mixing process is the bottleneck within the processing steps having an high impact on the overall system efficiency.

Due to the limitations of the single electrode circuit lines in the first design in a next step a matrix design of the electrowetting chip has been realized in order to achieve more flexibility concerning droplet processing. This offers the advantage of less electrode tracks and flexibility in verification of the theoretically modeled sorting routines. With this it is possible to handle and control droplets in parallel achieving the requested droplet generation of cell suspension and PBS dilution buffer and parallel mixing and splitting of droplets.

Additionally the electrode geometry is further optimized to a spline geometry as shown in Image 7. Due to this geometry the droplet is slightly overlapping the neighboring electrode which is improving each single required sorting step resulting in an overall improvement of the sorting speed. Furthermore the matrix design allows the droplet separation from one droplet directly into four droplets providing directly four droplets for the further processing concerning dilution and mixing followed by a next separation step.

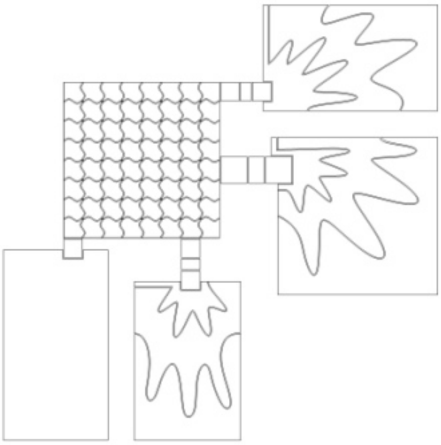


Image 7 Spline design of electrodes in matrix chip

3.2 On realistic sorter topologies

As the PBS supply and the removal of the end products have to be arranged around the main droplet flows, the throughput of a realistic sorter topology is expected to significantly drop (probably by one order of magnitude). The *lane sorter* depicted in Image 8 is supposed to provide a counterbalance to these bottlenecks due to scalability (and cascadability) even for a limited matrix consisting of $70 \times 11 = 770$ active electrodes. Here the cell suspension is arranged along path (A) where the droplets are divided and rearranged after being refilled from a counter-propagating PBS supply (B). As described above the refill of droplets always requires an additional mixing operation that is carried out by multiple circular movements over four electrodes, reducing the overall performance by 33%. The end products are removed laterally and introduced into the two output pathways (C). Typical benchmarks (for 100% sorter efficiency) yield a throughput (with respect to the end products) for one *lane sorter* unit in the order of 0.2 cells/clock, that scales worse with increasing path length (> 70) due to the imposed latency by the two "serial" PBS supplies. It's worth mentioning that the throughput can be significantly enhanced at the expense of lower efficiencies

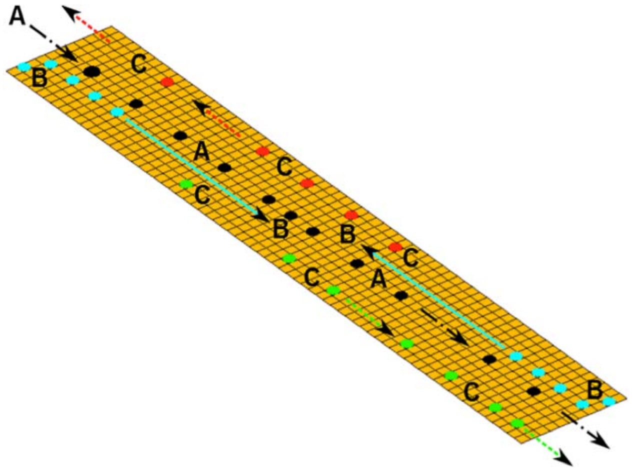


Image 8 Schematic of the scalable *lane sorter* unit with the cell suspension (A), PBS supply (B), and end products (C) with labeled cells (green) and residual cells (red).

To decrease the latency a novel *circulation sorter* has been proposed (Image 9) that was inspired by the concepts of various distribution network topologies [6]. The sorter architecture has a footprint corresponding to a 37 × 37 matrix encompassing only 590 active electrodes forming the corresponding channels. Here the PBS (C) is provided radially (in a parallel scheme) to the circulating droplet flow of the cell suspension (B). In comparison to the *lane sorter* we estimated a speed-up of the *circulation sorter* by a factor of two reaching a throughput of 0.4 cells/clock. Both realistic topologies show a ratio between transport clocks and manipulation clocks ranging up to 31:16, leaving room for further optimization. Hence, latency and the limited footprint turn out to be the major limitation on the sorter performance, may that be either throughput or sorter efficiency.

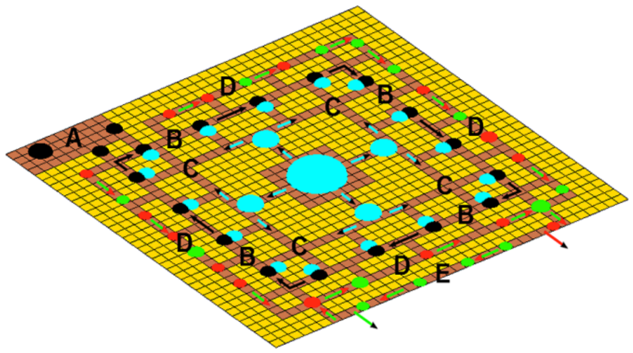


Image 9 Schematic of the *circulation sorter* with the suspension reservoir (A) and circulating channel (B), central PBS supply (C), end products (D) and output buffers (E).

4 Conclusions

Theoretical considerations have led to promising model topologies for the general cell sorting process. First tailored electrowetting chips confirmed the modeled process steps and timing required. This yields in a direct feedback to the modeling for further optimization of the final chip platform design for the later highly efficient sorting performance.

Regarding the sorter topology, two opposing design goals could be pursued, where the intended performance is on one hand defined as high-volume throughput with respect to the end products, and on the other hand as high sorting efficiency. A high sorting efficiency means that the cell suspension is completely itemized in the corresponding end products, namely the labeled cells and the residual cells. As an entry point to our presented design studies we have decided to maximize the sorting efficiency. From a theoretical point of view this is more challenging, because here the physical sorting algorithm is substantially relying on information processing issues, whereas a high throughput strongly hinges on the processing speed of the underlying manipulation operators. It seems that "smart" sorting has to be traded against "fast" sorting, or the sorting quality against the sorting quantity. In our case we will relax this trade-off by proper spatial scaling (i.e. parallelization) and cascading as well as by the careful enhancement of the electrowetting hardware. As next steps a larger electrode array chip will be build in order start testing the theoretically modeled process routines.

5 Acknowledgements

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